ME(EC Examination)

ET 542: Digital Systems Design

Time: Three hours 13 0 NOV 2016 Marks: 60

1. Solve any four questions
2. Figures to the right indicate full marks
3. Assume suitable data if necessary.
4. Use of nonprogrammable calculator is allowed.

Q. 1 A sequential circuit has two flip flops say A and B, two inputs say X and Y and an output z. The flip flop input functions and the circuit output functions are as follows: 15

$J_A = XB + \overline{Y}\,\overline{B}$, $J_B = XA$, $K_A = X\overline{YB}$, $K_B = X\overline{Y} + A$, $z = XYA + \overline{X}\,\overline{Y}\,B$

Construct a state table and a state graph. Show timing trace for values of flip-flops and output as far as possible. Assume initial value of each flip-flop as zero.

Q. 2 a) Write a VHDL code for an 8-bit register built with D-type flip flop, asynchronous clear, positive edge triggered with parallel-in parallel-out using generics 7

Q. 2 b) Write VHDL code for 8:1 multiplexer using "case" statement. 8

Q .3 a) Describe differences between transport delay and inertial delay with suitable examples. What do you mean by Simulation deltas ? 7

Q .3 b) Draw diagram of 3-input LUT. Determine the bits to be stored in the storage cells to realize the logic function $f = \overline{x_1}\overline{x_2}x_3 + \overline{x_1}x_2\overline{x_3} + x_1\overline{x_2}\overline{x_3} + x_1x_2x_3$ 8

Q. 4 a) Find the reduced PLA table to realize the following functions. 10

$F_1 = \sum m\,(2,3,5,7,8,9,10,11,13,15)$,

$F_2 = \sum m\,(2,3,5,6,7,10,11,14,15)$ and

$F_3 = \sum m\,(6,7,8,9,13,14,15)$

Write VHDL code for implementation of F_1, F_2 and F_3

Q. 4 b) Draw and explain architecture of Xilinx 9500 CPLD. 5

Q. 5 a) Discuss ones count and transition count compression technique. 8

Q.5 b) What is BIST? Explain types of BIST. Discuss the various techniques for test pattern generation. 7